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Computer Simulation of a Digital, One-Bit based, Balanced Quadricorrelator Applied to Multi-Level FSK Demodulator

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Abstract

PLL based frequency detectors have limited capabilities to properly demodulate FM signals (analog or digital) when the SNR is highly non-stationary (i.e. mobile). In order to solve this problem, we propose to use a ″One-Bit″ based balanced quadri-correlator (OBBQC) as frequency detector. Featuring a 100% ″multiplication-free″ structure, our design easily fits into "small size" FPGA's. It is highly flexible in the sense that one single "chip" will easily accommodate various FM modulation standards. It compares very well with other PLL's based, FM detectors [1,5,7].

1. Introduction

The digital frequency modulation (FSK, MLFSK, MSK, GMSK.) detectors play an important role in today's FM receivers. Unlike analog and digital phase detectors (commonly used in PLL's and DPLL's), there has been relatively little published on the performances of frequency detectors. From some available references [2,3], it appears that when these systems have to perform well in rather noisy environments (Gaussian, impulsive and non-stationary), the PLL based frequency detector may not behave well enough (temporary loss-of-lock, limited bandwidth…). The balanced quadri-correlator operating as frequency detector appears to overcome these limitations. Moreover, its structure lends itself very well to a "One-Bit" based DSP implementation [6]. This has the added advantages of being both inexpensive while performing well, at reasonable cost, in either low-power consumption designs or high frequency applications.

In a series of computer simulations (running under SystemView) and in comparisons with standard FM and/or FSK detectors [1,4,5,7], this approach presents promising results as well as a high degree of flexibility, since it benefits from the availability of quick programmable logic chips (i.e. FPGA).

Three different test signals, each of them with carrier frequencies of 10.7 MHz, were used to evaluate the performances of our realization of the OBBQC. They have the following properties:

Modulation type: **4 levels FSK**
Maximum Freq. Deviation: ± 200 KHz
Symbol rate: 256K/s
Nbr bits per symbols: 2 ➔ 512Kbits/s

Modulation type: **16 levels FSK**
Maximum Freq. Deviation: ± 240 KHz
Symbol rate: 128K/s
Nbr bits per symbols: 4 ➔ 512Kbits/s

Modulation type: **GMSK**
Maximum Freq. Deviation: ± 64 KHz
Bit rate (1/Tb): 256Kbits/s
Gaussian LPF: fc = 0.5/Tb = 128 KHz

The main features of the designs are:

- Multiplication-free low-pass filters approximated by zero-order hold (ZOH) functions.
- Three hard-limiters, one of which is positioned at the input of the quadricorrelator (before the mixers) and the two others after each of the two arm low-pass filters.
- The differentiators are replaced by delays.
- The local mixing frequency is purposely offset in such a way that the minimum

detected frequency is always larger than a given minimal value. This dramatically simplifies the filtering of the output waveform, which is in the form of a variable duty-cycle square-wave.

The primary challenge of this work was to design multiplication-free low-pass filters or averager functions, which would work reasonably well. One solution to this problem is to take the advantage of the fact that the ZOH function. It exhibits this desired low-pass filter characteristic, and it can be implemented with one integrator, one delay and one substractor. However, in practice, there is always a DC component added to the AC at the integrator input. This will bring its output to drift and, eventually, to either go into "saturation mode" or "numeric overflow". Therefore, a slightly different approach must be used. It appears that two separate integrators adequately coupled with threshold detectors and simple arithmetic functions provide a very good solution to this problem.

A concrete design has the following specifications:

Modulation type: **4 levels FSK (4LFSK)**
Clock Frequency: 40.8 MHz
Decimation Factors: 4
Mixer Offset Freq. (foffset): 500 KHz
Nbr. Unit Delays (D Flip-Flops): 210
Max. Freq. Deviation: ± 200 KHz:
Maximum Bit Rate: 512 Kbits/s

The framework of this paper is as follows: in section 2, we present the basic principle of the OBBQC, with typical plots of its main signals. Then, in section 3, the averagers, or ZOH functions, are discussed and, the chosen implementation scheme presented. In section 4, computer simulations presenting eye-diagrams, with and without additive Gaussian noise are shown as well as non-stationary conditions (i.e. varying SNR and burst transmission). The **GMSK** case is also considered and the performances of the OBBQC compared with theoretical results. Finally, the last section summarizes the advantages of this design and suggests potential improvements and applications.

2. OBBQC BASIC PRINCIPLE

Fig. 1 shows the basic bloc diagram of the OBBQC, Fig. 2 depicts its main signals. The input signal (coming from the receiver IF output) is a FSK type signal (± 200 KHz of deviation, no noise). Tokens 14, 15, 16 and 17 are "one-bit" multipliers (XORs) while tokens 9, 10, 11 and 19 are averagers acting as simplified low-pass filters. It is well known that an averager is nothing else than a ZOH function.

From straightforward analysis [2], the average value of the adder's output (token 2) is proportional to the frequency deviation (in the form of a variable duty-cycle!). This is clearly illustrated in Fig. 2 (bottom right trace). In other words, that is the amplitude of the modulating signal. The frequency of token 2 output is determined as follows: $4 * (foffset + fdev)$, where foffset = 10.7 MHz – 10.2 MHz = 500 KHz. The combined tokens 11 and 19 produce the running average of token 2 output, therefore, token 12 input (Fig. 2, bottom left trace) is directly the modulating signal amplitude (the averaging time of AVER3 and AVER4 are adapted to the symbol rate of the modulating signal). The decimation (token 18) is optimized with each specific modulation type (factor 2 to 8).

AVER1 and AVER2 (Fig.2, top left trace) main functions are to filter out the sum of both the input signal frequency and the generator frequency. The cut-off frequencies of these filters are matched to the bandwidth of the incoming 4LFSK signal. Note that their respective outputs are in quadrature. Tokens 1 and 4 are delays. They advantageously (in a practical realization) replace, with little degradation, the differentiator's functions that we find in the original design [2].

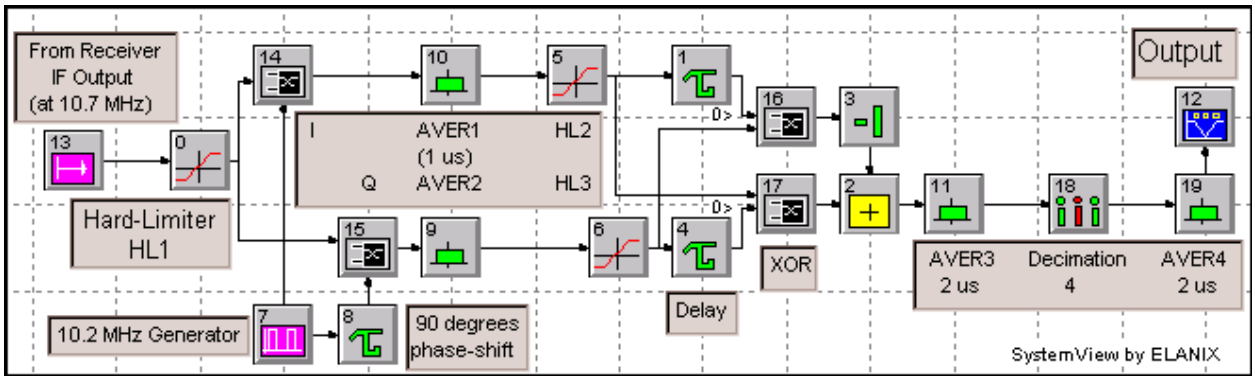

Figure 1: OBBQC basic bloc diagram

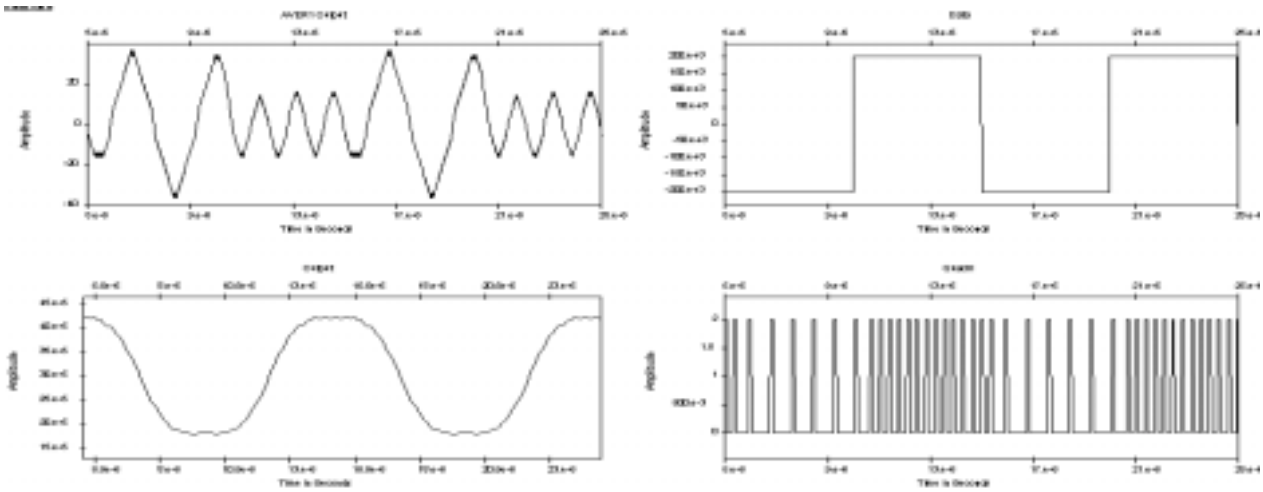

Figure 2: Aver1 (top left), Data (top right), Quadri(bottom right), Output (bottom left)

3. AVERAGER BLOC DIAGRAM

The principle of the averager is shown in Fig. 3.

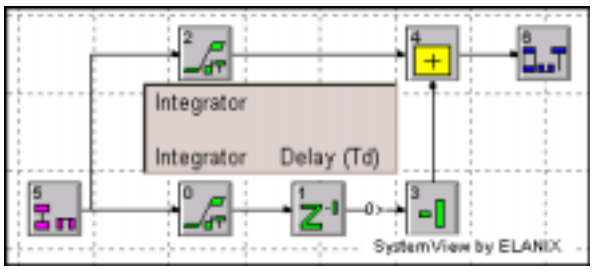

Figure 3: Principle of the averager.

This solution is chosen since the input waveform of all but one averager (Token 19) are “One-Bit” signals. This minimizes the number of unit delays (D-flip-flops). The complete averager bloc diagram is presented in Fig.4. It is made out of two separate integrators (Tokens 1,10 and 4,11). The output of the first integrator (INT1) goes to a threshold detector (Token

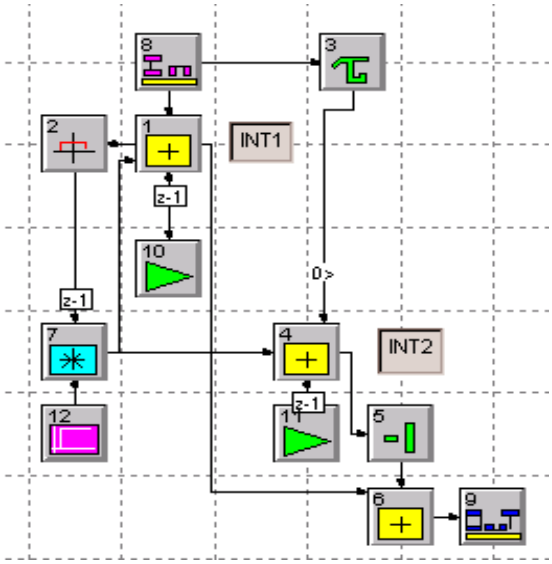

Figure 4: Averager Implementation

2). Whenever INT1 absolute value is larger than a preset value, this last one is simultaneously subtracted (or added) from both integrators, thus avoiding overflow (or underflow). Token 3, a delay, is the averaging time of this running averager. It is the most critical part of this design since the sum of the gates used to synthesize all the delays represents more than 80% of the total "gate count".

4. COMPUTER SIMULATIONS

4.1 EYE DIAGRAMS

Eye diagrams are used to show the performances of the OBBQC with the three selected test signals. Note that the low-pass filtering (AVER3 and AVER4) is not optimized and that additional spectral shaping is required. In the case of the GMSK, the addition of a simplified Gaussian LPF (made out of three averagers, two delays and one adder) produces a real improvement (in the order of 1.5 to 2 dB) that can be easily seen when comparing Fig. 9 and 10.

4.11 4 levels FSK

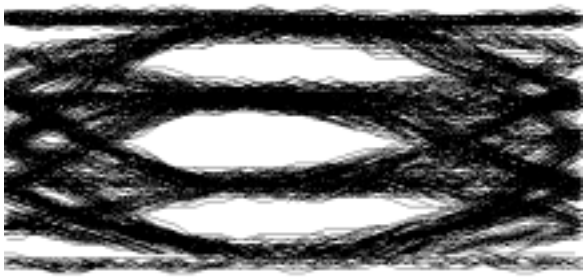

Figure 5: Eb/No > 40 dB.

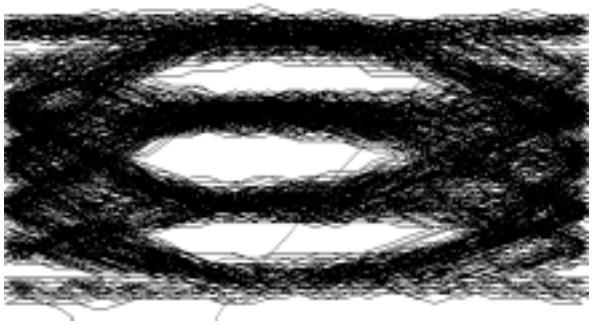

Figure 6: Eb/No = 19 dB

4.1.2 16 levels FSK

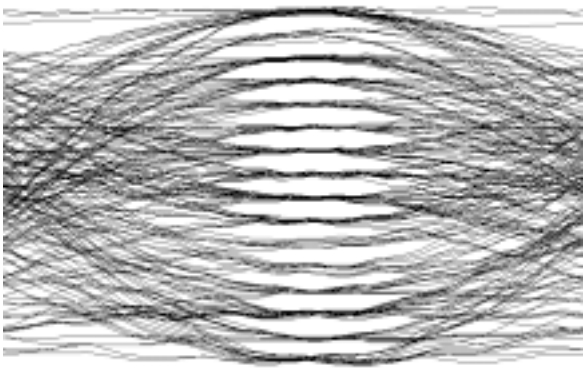

Figure 7: Eb/No > 40 dB.

4.1.3 GMSK

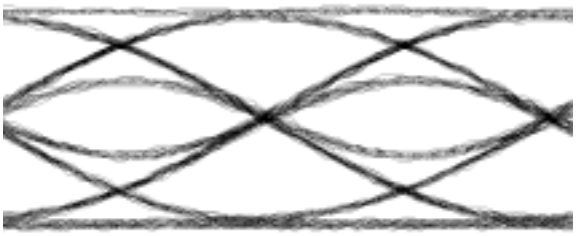

Figure 8: Eb/No > 40 dB.
(No Gaussian LPF)

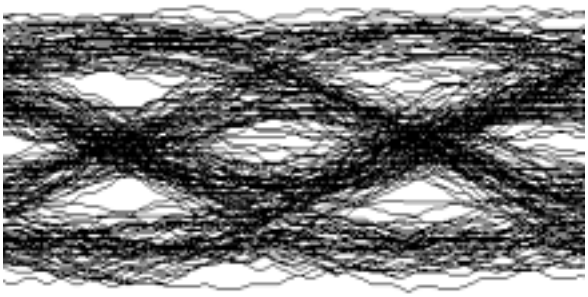

Figure 9: Eb/No = 12 dB.
(No Gaussian LPF)

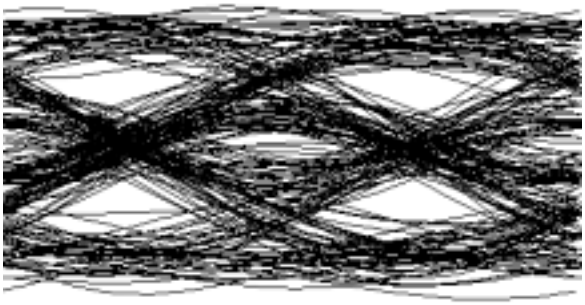

Figure 10: Eb/No = 12 dB
(Gaussian LPF).

The comparison with the theoretical result [7] shows a total degradation of approximately 4 dB as compared with the optimum GMSK receiver. However, if the noise is non-stationary and/or impulsive, this design is very competitive and would, in some cases, outperform a "regular" approach. The estimated number of flip-flops is of 1000.

4.2 NON-STATIONARY SNR

In Fig. 11 and 12, we use a burst type, 4-levels FSK modulation, to test the "robustness" of the OBBQC under strong SNR variation (30 dB). As seen in Fig. 12, the recovery of the modulating signal is perfect as soon as the SNR goes above a given threshold.

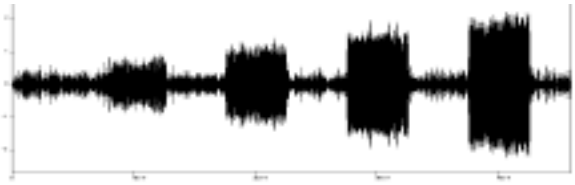

Figure 11: 4LFSK Signal + Noise.

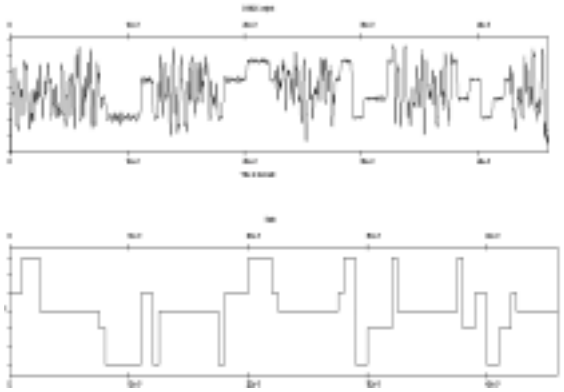

Figure 12: Mod. Signal (bottom), Recovered Mod. (top).

5. CONCLUSIONS

The extensive computer simulations and the performance comparisons with PLL based detectors have shown that this OBBQC, performs very well under a large variety of SNR conditions and/or transmission modes. Moreover, it does not have the usual drawbacks of the PLLs (loss-of-lock, acquisition time…). In addition to that, the relatively low clock frequency and small number of unit delays (D-FFs) used, makes the OBBQC a good candidate for high speed applications (i.e. digital links in the Mbits/s range), burst type digital transmissions (no acquisition time) or ultra-low power requirement (at low carrier frequency). Other challenging applications, such as: Digital Phase/Frequency Locked-Loop and Double Quadri-Correlator will be considered in the future.

6. SAMPLE REFERENCES

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